

DARPA-BAA-15-55 (CRAFT) FAQ

Summary of Questions:

1. **Q: Will the government deliver packaged parts? Are you delivering full wafers or bare dies?**
A: DARPA plans to provide die only.
2. **Q: Could you clarify 3rd party IP. Is it reusable IP or IP purchased from outside the company?**
A: Third party IP is IP obtained from outside of the proposing team.
3. **Q: For the cost proposal, how would you like us to handle the cost of 3rd party IP?**
A: Include in your proposal the cost of all 3rd party IP required to build the SoCs you plan to design as part of your proposal.
4. **Q: Should the cost of 3rd party IP and EDA tools be included in the cost proposal?**
A: Yes, EDA tools, IP, etc. required to implement the proposer-based designs should all be included in the cost proposal.
5. **Q: Given different platforms, how do you gauge success?**
A: Please review the deliverables and metrics outlined in the BAA, beginning on page 8. The design flow developed in TA1 will be compared to the effort required to design the same integrated circuit using the current ASIC design flow. The port and migrate flows developed in TA2 will be compared to the effort required to design the same integrated circuit using the CRAFT designed flow from TA1.
6. **Q: Does design cycle include fab cycle?**
A: Design cycle starts with design start with top level architecture defined and ends with delivery of GDS for fabrication.
7. **Q: How do we establish a baseline design cycle time?**
A: The baseline design cycle time is defined as the amount of time (effort) required to design the integrated circuit using today's commercial flows and methods.
8. **Q: Is the repository taking feeds from TA1 and TA2?**
A: Yes. Please refer to pages 9, 12, and 14 where the BAA explicitly requires that TA1/TA2 teams provide inputs to the repository and that the repository support TA1/TA2 teams.
9. **Q: Are proposers required to submit to the first MPW shuttle run?**
A: No, proposers are not required to submit to the February 2016 MPW shuttle run.
10. **Q: Are fabrication costs a separate line item in the cost proposal?**
A: Proposers should not include die fabrication costs in their proposals, but should include an estimate of required fabrication area. Fabrication for CRAFT performers will be provided separately by DARPA.
11. **Q: Are we expected to have hardware at the end of Phase 1?**
A: You are not expected to have hardware at the end of Phase 1. Program evaluation at the end of phase 1 will be based on simulation results.
12. **Q: Will there be a down-selection enabled through the design challenge?**

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A: No, please refer to table 1 in the BAA on page 17 for details of the selection criteria. Phase I and Phase II will have design evaluation activities and only Phase III will have a design challenge.

13. Q: How much of the flow will be provided to designers in TA1 and TA2?

A: Each proposer will need to define all tools required to implement their design flow and indicate a plan for other teams to obtain those tools.

14. Q: How do you plan to incorporate port/migrate in the shuttle runs?

A: DARPA will pay for area on foundry-provided MPW runs at the DARPA-selected secondary foundry and at the DARPA-selected secondary technology node.

15. Q: Do you anticipate TA1 to be a tool development effort?

A: Yes, proposers should propose development of the tools necessary to achieve the goals of the program. DARPA anticipates that at least some EDA tool development will be required.

16. Q: Do you anticipate regrouping of teams during the program?

A: No

17. Q: Can proposers pay for a separate MPW on their own and use another foundry?

A: No, CRAFT will not provide support for separate runs.

18. Q: Do the final deliverables include vendor supplied tools?

A: No, proposers should deliver all tools developed in this program. If the flow requires use of existing EDA vendor tools, that should be explicitly indicated in the proposal and in the description of the final deliverables.

19. Q: When you use the terminology flow, do you mean documentation or software?

A: EDA tools, software tools purchased from third party, and documentation of how others can use the flow.

20. Q: Will the evaluation team evaluate multiple designs?

A: The evaluation team will design at least one integrated circuit as part of the Phase II evaluation.

21. Q: What should be the handoff in Phase 2?

A: Deliverables and metrics are in the BAA on pages 9 through 17.

22. Q: Who will the evaluation team be?

A: The evaluation teams will be determined during Phase 1 of the program.

23. Q: Will the slides shown at the CRAFT Proposers Day be made available to proposers?

A: Yes, slides presented at the CRAFT Proposers Day are available on DARPA.mil.

24. Q: Are the shuttle runs open to all government programs?

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A: Although this question does not apply to proposals submitted to the CRAFT BAA, DARPA will fund the shuttle runs and they are open to government programs. Government programs, other than CRAFT, will need to pay for fabrication area.

25. Q: Should CRAFT proposers include fabrication costs in their cost proposals?

A: As stated on page 8 of the BAA, “DARPA will provide fabrication support through a number of separately funded multi-project runs and therefore, fabrication costs should not be included in proposal budgets.” However, proposers should indicate the amount of fabrication area that will be required to meet the goals for their proposed work.

26. Q: Are you going to recommend a vendor for EDA tools?

A: No, Proposers should include an EDA tool scenario in their technical and cost proposals. The scenario should be for the optimal EDA tool suite needed for the proposed program. Proposers should ensure that the costs are clearly defined in the proposal.

27. Q: How do I get access to 3rd party IP?

A: Each proposer should include a plan and costs for the 3rd party IP required to for the proposed program.

28. Q: There appears to be a contradiction between not needing a new language but needing object oriented design (OOD).

A: There is no contradiction. The BAA states on page 7 the need for a new design flow. Proposers should propose the activities necessary to meet the program metrics.

29. Q: In the BAA it mentions "Logic block size of > 200k gates." Does this imply sub-components > 200K gates or complete SOC designs that are > 200K gates?

A: As stated in the BAA on page 9, the logic gate count in the SOC is larger than 200k gates for Phase 1. The total gate count is expected to be much larger when memory, analog and other pieces of the SoC are included for phase 1. Note that the logic block size of > 200k gates is a minimum for performer-provided designs only in Phase I. Proposers should expect that the DARPA-provided designs in Phases II and III will have logic gate counts of more than 200M gates, tens of analog blocks, extensive memory requirements, and multiple instances of 3rd party IP. It is critical that proposers do not confuse the relatively low complexity targets for Phase I with the much higher complexity targets for the rest of the program.

30. Q: Are there any suggested SOC designs for the Phase I effort?

A: As stated in the BAA on page 9, each proposal should include a plan for a proposer-provided SoC in Phase I. Proposals will be evaluated not only on the likelihood of technical success, but also on the complexity of the performer-defined SoC used for that evaluation.

31. Q: Should we include memory generators as part of this effort or should be assume memory generators will available?

A: As stated in the BAA on pages 9 and 16, proposers should include the memory components required for successful design of proposer-defined and future DARPA-defined SoCs.

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32. Q: TA3 question: Does the proposer have to designate where the repository will be housed long-term or will the Government do that? It would seem that a proposer who has the capability to develop the secure procedures needed to setup and establish all the cyber security and content distribution aspects of the repository would be at a disadvantage compared to one who already has a relationship with the Government (e.g. an FFRDC) and thus can propose to house the repository.

A: The CRAFT BAA indicates the following required deliverables:

- “A plan for continuation and sustainability of the repository after program completion” (Phase I on page 14)
- “Implementation of the plan for continuation and sustainability of the repository after program completion” (Phase III on page 15)

33. Q; Table 1, BAA pg 17: per proposer’s day comments regarding the first 16/14nm MPW fab run (~Feb-2016), do we ignore the initial hardware generator/macro test results requirement for TA1-Phase1? (and, does that requirement now move to TA1-Phase2)

A: Proposers may expect to have hardware results from a Fall, 2016 shuttle run.

34. Q: Table 1, BAA pg 17: for TA1-Phase2, isn’t the performer also a designer for the DARPA-selected custom IC?

A: No, the designer of the evaluation design will be the DARPA-formed evaluation team. Performer-designed hardware will also be evaluated as part of the program.

35. Q: BAA pg 10: for TA1-Phase3, isn’t the performer also a designer for the DARPA Open Design Challenge? If not, why is that design listed as a deliverable on page 10?

A: No, the performer will not be a participant in the Open Design Challenge. However, as noted on page 10 of the BAA, “Performers are also expected to provide their design flow and support to a group of independently funded teams who will design multiple DoD-specific custom integrated circuits that will be fabricated, and confirmed through hardware testing.”

36. Q: TA1-Phase3 Open Design Challenge: is fabrication and test (hardware verification) expected to be completed in Phase3? Or, is the Open Design Challenge a paper design only?

A: As noted in Table 1 of the BAA on page 17, the results of the Open Design Challenge will be evaluated based on simulation results and not on hardware test results. This is mandated by the shuttle run schedules.

37. Q: What is the status of releasing foundry selection and PDK information for the technologies to be used for the CRAFT program? (this information impacts our ability to line up 3rd party IP and other details of our proposal)

A: Proposers should provide a proposal that is independent of the chosen foundry. Please also refer to FAQ question #25.

38. Q: For TA2, are we correct in assuming that both the performer-selected (Phase 2) and DARPA-selected (Phase3) SoC designs are functionally identical to the ones from TA1 (such that the task is focused solely on demonstrating the porting and migrating flows, and not creating a diversity of SoC designs)?

A: Yes, the SoC designs may be functionally identical.

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39. Q: Page 9 of the BAA states that “At the conclusion of Phase I, performers should have demonstrated a 10X reduction in the design effort required to create a design using a standard flow for an SoC of their choosing”, while Page 16 states that a “5X reduction” is required at the conclusion of Phase I. Is this a contradiction, or am I reading the BAA incorrectly for TA1, Phase 1.

A: This is not a contradiction. The 10X reduction on page 9 refers to the proposer-selected design. The 5X reduction on page 16 refers to a representative DoD design.